RD74VT1G240

Bus Buffer Inverted with 3-state Output / Dual Supply Voltage Translator

REJ03D0518-0100 Rev.1.00 Jun. 01, 2005

Description

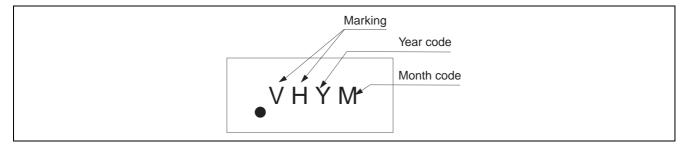
The RD74VT1G240 has a bus buffer inverted with 3-state output in a 6 pin package. Output is disabled when the associated output enable (\overline{OE}) input is high. To ensure the high impedance state during power up or power down, \overline{OE} should be connected to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver. The input is designed to track V_{CC} IN, which accepts voltages from 1.2V to 3.6V, and the output is designed to track V_{CC} OUT, which operates at 1.2V to 3.6V. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

- This product function as level shift that change $V_{CC}IN$ input level to $V_{CC}OUT$ output level by providing different supply voltage to $V_{CC}IN$ and $V_{CC}OUT$.
- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- Supply voltage range: $V_{CC}IN = 1.2 \text{ V to } 3.6 \text{ V}$ $V_{CC}OUT = 1.2 \text{ V to } 3.6 \text{ V}$ Operating temperature range: -40 to +85°C
- All inputs V_{IH} (Max.) = 3.6 V (@V_{CC}IN = 0 V to 3.6 V) Outputs V₀ (Max.) = 3.6 V (@V_{CC}OUT = 0 V)
- Output current $\pm 2 \text{ mA} (@V_{CC}OUT = 1.2 \text{ V})$ $\pm 4 \text{ mA} (@V_{CC}OUT = 1.4 \text{ V} \text{ to } 1.6 \text{ V})$ $\pm 6 \text{ mA} (@V_{CC}OUT = 1.65 \text{ V} \text{ to } 1.05 \text{ V})$
 - $\pm 6 \text{ mA}$ (@V_{CC}OUT = 1.65 V to 1.95 V) $\pm 18 \text{ mA}$ (@V_{CC}OUT = 2.3 V to 2.7 V) $\pm 24 \text{ mA}$ (@V_{CC}OUT = 3.0 V to 3.6 V)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
RD74VT1G240CLE	WCSP-6 pin	SXBG0006KB–A (TBS-6AV)	CL	E (3,000 pcs/reel)

Article Indication





Function Table

Inp	uts	
ŌĒ	А	Output Y
L	L	Н
L	Н	L
Н	Х	Z

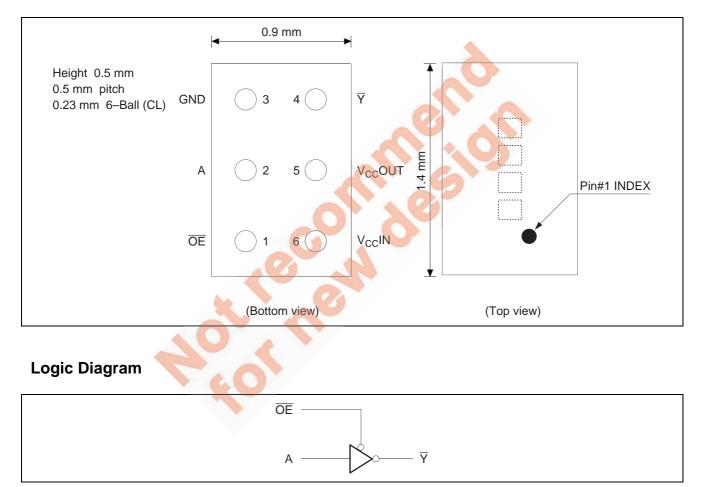
H: High level

L: Low level

X: Immaterial

Z: High impedance

Pin Arrangement





Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V _{CC} IN, V _{CC} OUT	-0.5 to 4.6	V	
Input voltage range *1	VI	-0.5 to 4.6	V	A port or OE
Output voltage range *1, 2	Vo	-0.5 to V _{CC} OUT+0.5	V	Output: "H" or "L"
		-0.5 to 4.6		Output: "Z" or V _{CC} OUT: OFF
Input clamp current	I _{IK}	-50	mA	V ₁ < 0
Output clamp current	I _{ОК}	-50	mA	V ₀ < 0
		50		$V_0 > V_{CC} + 0.5$
Continuous output current	Ιο	±50	mA	
Continuous output current V _{CC} or GND	$I_{CC}IN$, $I_{CC}OUT$, I_{GND}	±100	mA	
Package Thermal impedance	θ_{ja}	123	°C/W	
Storage temperature	Tstg	-65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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2. This value is limited to 4.6 V maximum.

Recommended Operating Conditions

ltem	Symbol	Ratings	Unit	Conditions
Supply voltage range	VccIN	1.2 to 3.6	V	
	V _{cc} OUT	1.2 to 3.6		
Input/Output voltage	VI	0 to 3.6	V	A port or OE
	Vo	0 to V _{cc} OUT	V	Output: "H" or "L"
		0 to 3.6		Output: "Z" or V _{CC} OUT: OFF
Output current	Іон	-2	mA	$V_{CC}OUT = 1.2 V$
		-4		$V_{CC}OUT = 1.5 \pm 0.1 V$
		-6		V _{CC} OUT = 1.8±0.15 V
		-18		$V_{CC}OUT = 2.5 \pm 0.2 V$
		-24		$V_{CC}OUT = 3.3\pm0.3 V$
	I _{OL}	2	mA	$V_{CC}OUT = 1.2 V$
		4		V _{CC} OUT = 1.5±0.1 V
		6		V _{CC} OUT = 1.8±0.15 V
		18		$V_{CC}OUT = 2.5 \pm 0.2 V$
		24		V _{CC} OUT = 3.3±0.3 V
Input transition rise or fall time	$\Delta t / \Delta v$	10	ns / V	
Operation free-air temperature	Та	-40 to 85	°C	



Electrical Characteristics

 $(Ta = -40 \text{ to } 85^{\circ}\text{C})$

ltem	Symbol	V _{cc} IN (V) [*]	V _{cc} OUT (V) [*]	Min	Тур	Max	Unit	Test conditions
Input voltage	VIH	1.2	1.2 to 3.6	V _{CC} IN×0.75	_		V	A port
		1.5±0.1		V _{CC} IN×0.70	_			Control input
		1.8±0.15		V _{CC} IN×0.65	_			
		2.5±0.2		1.6	_			
		3.3±0.3		2.0	_			
	VIL	1.2	1.2 to 3.6		_	V _{CC} IN×0.25	V	A port
		1.5±0.1			_	V _{CC} IN×0.30		Control input
		1.8±0.15			_	V _{CC} IN×0.35		
		2.5±0.2			_	0.7		
		3.3±0.3			_	0.8		
Output voltage	Vон	1.2 to 3.6	1.2 to 3.6	V _{CC} OUT-0.2	—		V	I _{OH} = -100 µА
			1.2	0.9	_			I _{OH} = -2 mA
			1.5±0.1	1.1	_			I _{OH} = -4 mA
			1.8±0.15	1.25	_			I _{OH} = -6 mA
			2.5±0.2	1.7	_			I _{OH} = -18 mA
			3.3±0.3	2.2	_	G		I _{OH} = -24 mA
	V _{OL}	1.2 to 3.6	1.2 to 3.6			0.2	V	I _{OL} = 100 μA
			1.2			0.3		$I_{OL} = 2 \text{ mA}$
			1.5±0.1	—	- - 2 /	0.3		I _{OL} = 4 mA
			1.8±0.15			0.3		I _{OL} = 6 mA
			2.5±0.2	—		0.6		I _{OL} = 18 mA
			3.3±0.3	_	—	0.55		I _{OL} = 24 mA
Input current	I _{IN}	3.6	3.6	-1.0		1.0	μA	$V_{IN} = GND \text{ or } V_{CC}IN$ control input
Off state output current	I _{oz}	3.6	3.6	-1.5		✓ 1.5	μA	$V_{IN} = V_{IH}$ or V_{IL}
Output leakage current	I _{OFF}	0	0			1.5	μA	V _{IN} , V _{OUT} = 0 to 3.6 V
Quiescent supply current	I _{CC} IN	1.2 to 3.6	1.2 to 3.6	-3.0	_	3.0	μA	$I_{O(\overline{Y} \text{ port})} = 0$ V _{IN} = V _{CC} IN or GND
,	I _{CC} OUT	1.2 to 3.6	1.2 to 3.6	-3.0	—	3.0		$I_{O(\overline{Y} \text{ port})} = 0$ V _{IN} = V _{CC} IN or GND
Increase in I _{CC} per input	Δl _{cc}	3.6	3.6	—	—	250	μA	A port or control V _{CC} IN–0.6 (1 input)
Input capacitance	C _{IN}	3.3	3.3	—	3.5		pF	$V_{IN} = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

							Ta =	40 to 85	°C					
				V _{cc} OUT=	V _{cc} C	DUT=	V _{cc} C	DUT=	V _{cc} C)UT=	V _{cc} C	DUT=		
		From	То	1.2 V	1.5±	0.1 V	1.8±0).15 V	2.5±	0.2 V	3.3±	0.3 V		Test
ltem	Symbol	(input)	(output)	Тур	Min	Max	Min	Max	Min	Max	Min	Max	Unit	conditions
Propagation	t _{PLH}	А	Ŷ	9.6	2.0	9.4	1.0	6.0	1.0	4.0	1.0	3.4	ns	C _L = 15pF
delay time	t _{PHL}			9.6	2.0	9.4	1.0	6.0	1.0	4.0	1.0	3.4		$R_L = 2.0 k\Omega$
Output	t _{ZH}	ŌĒ	Ŧ	11.2	2.0	10.6	1.5	6.8	1.0	4.2	1.0	3.8	ns	C∟ = 15pF
enable time	t _{ZL}			11.2	2.0	10.6	1.5	6.8	1.0	4.2	1.0	3.8		$R_L = 2.0 k\Omega$
Output	t _{HZ}	ŌĒ	Ŧ	5.0	2.0	5.4	1.5	4.7	1.0	4.0	1.0	3.8	ns	C _L = 15pF
disable time	t _{LZ}			5.0	2.0	5.4	1.5	4.7	1.0	4.0	1.0	3.8		$R_L = 2.0 k\Omega$

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Switching Characteristics (Cont)

 $V_{CC}IN=2.5{\pm}0.2~V$

							Ta = -4	40 to 85	°C					
		From	То	V _{cc} OUT= 1.2 V		OUT= 0.1 V	00	OUT= 0.15 V	V _{cc} C 2.5±	0UT= 0.2 V		DUT= 0.3 V		Test
Item	Symbol	(input)	(output)	Тур	Min	Max	Min	Max	Min	Max	Min	Max	Unit	conditions
Propagation	t _{PLH}	А	Ŧ	10.0	2.0	9.4	1.5	6.0	1.0	4.0	1.0	3.5	ns	$C_L = 15 pF$
delay time	t _{PHL}			10.0	2.0	9.4	1.5	6.0	1.0	4.0	1.0	3.5		$R_L = 2.0 k\Omega$
Output	t _{ZH}	ŌĒ	Ŧ	11.6	2.0	11.4	1.5	7.2	1.0	4.8	1.0	3.8	ns	$C_L = 15 pF$
enable time	t _{ZL}			11.6	2.0	11.4	1.5	7.2	1.0	4.8	1.0	3.8		$R_L = 2.0 k\Omega$
Output	t _{HZ}	ŌĒ	Ŧ	5.2	2.0	5.0	1.5	4.7	1.0	4.0	1.0	4.0	ns	$C_L = 15 pF$
disable time	t _{LZ}			5.2	2.0	5.0	1.5	4.7	1.0	4.0	1.0	4.0		$R_L = 2.0 k\Omega$

 $V_{CC}IN = 1.8 \pm 0.15 V$

							Ta =	40 to 85	°C					
				V _{cc} OUT=	VccC	DUT=	VccC	DUT=	= V _{cc} OUT=		V _{cc} C	V _{cc} OUT=		
		From	То	1.2 V	1.5±	0.1 V	1.8±0.15 V		2.5 <mark>±0.2 V</mark>		3.3±0.3 V			Test
Item	Symbol	(input)	(output)	Тур	Min	Max	Min	Max	Min	Max	Min	Max	Unit	conditions
Propagation	t _{PLH}	А	Ŧ	10.2	2.0	9.8	1.5	6.5	1.0	4.4	1.0	4.1	ns	$C_L = 15 pF$
delay time	t _{PHL}			10.2	2.0	9.8	1.5	6.5	1.0	4.4	1.0	4.1		$R_L = 2.0 k\Omega$
Output	t _{ZH}	ŌĒ	Ŧ	11.6	2.0	11.8	1.5	7.6	1.0	5.2	1.0	4.4	ns	$C_L = 15 pF$
enable time	t _{ZL}			11.6	2.0	11.8	1.5	7.6	1.0	5.2	1.0	4.4		$R_L = 2.0 k\Omega$
Output	t _{HZ}	ŌĒ	Ŧ	5.8	2.0	5.6	1.5	5.4	1.0	4.8	1.0	5.0	ns	$C_L = 15 pF$
disable time	t _{LZ}			5.8	2.0	5.6	1.5	5.4	1.0	4.8	1.0	5.0		$R_L = 2.0 k\Omega$

 $V_{CC}IN = 1.5\pm0.1 V$

				.0	$\boldsymbol{\lambda}$		Ta =	40 to 85	°C					
				V _{cc} OUT=	V _{cc} C	DUT=	V _{cc} C	DUT=	V _{cc} C	DUT=	VccC	DUT=		
		From	То	1.2 V	1.5 <u>+</u>	0.1 V	1.8±0).15 V	2.5±	0.2 V	3.3±	0.3 V		Test
ltem	Symbol	(input)	(output)	Тур	Min	Max	Min	Max	Min	Max	Min	Max	Unit	conditions
Propagation	t _{PLH}	A	Ŷ	11.4	2.0	10.5	1.5	7.2	1.0	4.8	1.0	4.7	ns	$C_L = 15 pF$
delay time	t _{PHL}			11.4	2.0	10.5	1.5	7.2	1.0	4.8	1.0	4.7		$R_L = 2.0 k\Omega$
Output	t _{ZH}	ŌĒ	Ŧ	12.2	2.0	12.6	1.5	8.6	1.0	5.4	1.0	4.8	ns	$C_L = 15 pF$
enable time	t _{ZL}			12.2	2.0	12.6	1.5	8.6	1.0	5.4	1.0	4.8		$R_L = 2.0 k\Omega$
Output	t _{HZ}	ŌĒ	Ŧ	6.2	2.0	7.0	1.5	6.0	1.0	5.4	1.0	5.2	ns	$C_{L} = 15 pF$
disable time	t _{LZ}			6.2	2.0	7.0	1.5	6.0	1.0	5.4	1.0	5.2		$R_L = 2.0 k\Omega$

 $V_{\rm CC}IN = 1.2 \ V$

					Т	a = –40 to 85°	С			
				V _{cc} OUT=						
		From	То	1.2 V	1.5±0.1 V	1.8±0.15 V	2.5±0.2 V	3.3±0.3 V		Test
ltem	Symbol	(input)	(output)	Тур	Тур	Тур	Тур	Тур	Unit	conditions
Propagation	t _{PLH}	А	Ŧ	11.0	7.5	6.0	4.5	4.0	ns	$C_L = 15 pF$
delay time	t _{PHL}			11.0	7.5	6.0	4.5	4.0		$R_L = 2.0 k\Omega$
Output	t _{ZH}	ŌĒ	Ŷ	12.8	9.5	7.2	5.2	4.5	ns	$C_L = 15 pF$
enable time	t _{ZL}			12.8	9.5	7.2	5.2	4.5		$R_L = 2.0 k\Omega$
Output	t _{HZ}	ŌĒ	Ϋ́	7.0	6.0	5.7	5.5	5.5	ns	$C_L = 15 pF$
disable time	t _{LZ}			7.0	6.0	5.7	5.5	5.5		$R_L = 2.0 k\Omega$



Operating Characteristics

 $Ta = 25^{\circ}C$

ltem	Symbol	V _{cc} IN (V)	V _{cc} OUT (V)	Min	Тур	Max	Unit	Test conditions
Power dissipation	CPD	3.3	3.3	_	12		pF	f = 10 MHz
capacitance								$C_L = 0$

Power-up Considerations

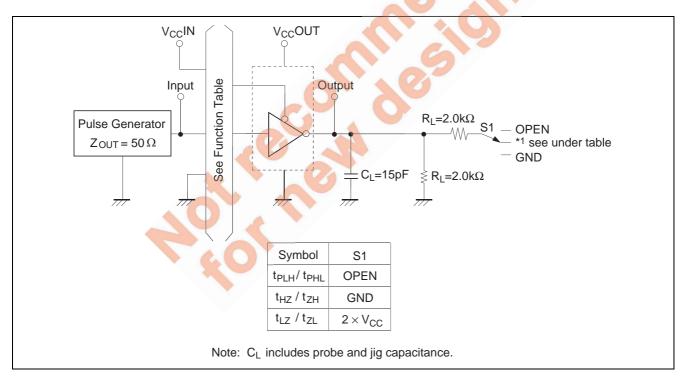
Level-translation devices offer an opportunity for successful mixed-voltage signal design.

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins.

Take these precautions to guard against such power-up problems.

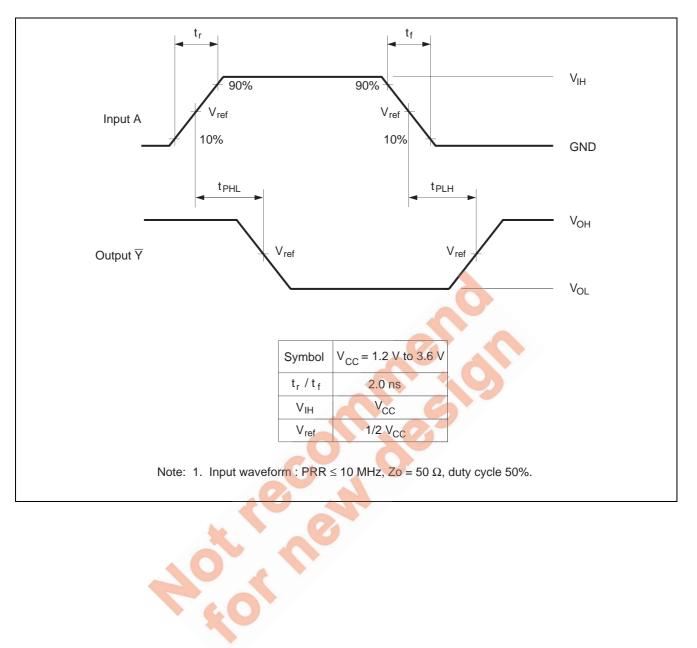
- 1. Connect ground before any supply voltage is applied.
- 2. Next, power up the control side of the device.
- (Power up of V_{CC} IN is first. Next power up is V_{CC} OUT)
- 3. Tie \overline{OE} to V_{CC}IN with a pull-up resistor so that it ramps with V_{CC}IN.





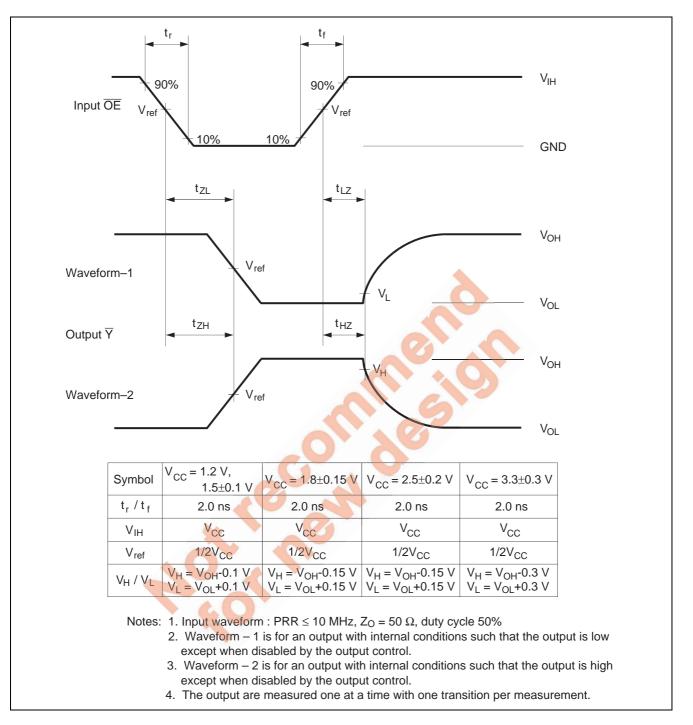


Waveforms-1



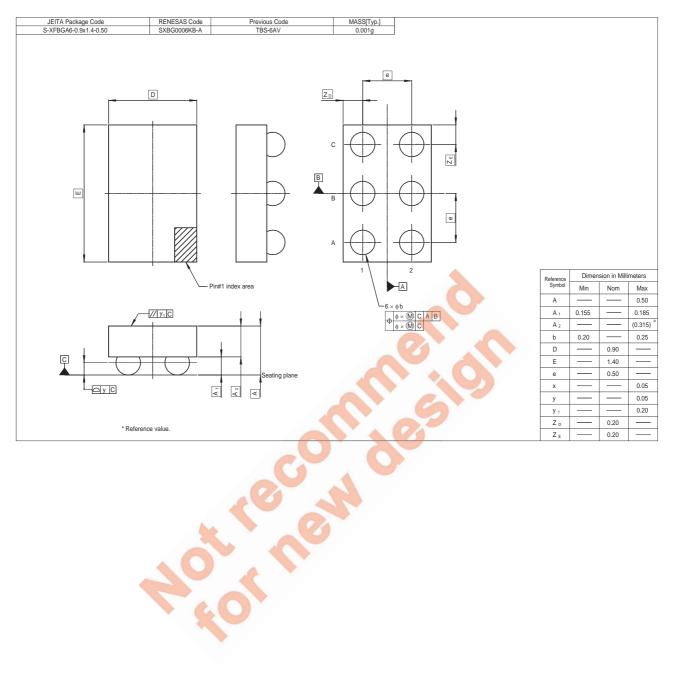


Waveforms-2





Package Dimensions





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